Developing Protective Limiters for a Hydro Power Controller in Modelica

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Abstract

In recent years the operation of electrical power plants has become more and more challenging due to a more dynamic operation pattern in order to keep the voltage quality within the limits of what the electrical network regulators allow. This is due to the ever increasing amount of unregulated renewable energy (e.g., wind, solar, tidal power). There is a need for better tools that allow for a better and more accurate simulation of the operation of a electrical power plant. This paper presents the development of protective limiters as used in a typical hydro power controller. The limiters have been implemented using the Modelica language (Modelica Association 2017) and are according to the IEEE Std 421.5-201 (IEEE 2016). Having the limiters available in Modelica makes it possible to integrate them with hydro power system models build with the use of OpenHPL (TMCC 2019). The behaviour of the limiters have been tested against a verified generator model of the OpenIPSL (ALSETLab et al. 2018) comparing the theoretical behaviour.

Keywords: hydro power, Modelica, excitation system, protective controller, limiter

1 Introduction

The electrical power demand is still increasing, and it leads to pushing the society to find a renewable source to produce electricity. Therefore the development of existing and new hydropower stations is still increasing. The development of hydropower plants focuses not only on larger hydropower plants but also on small-scale hydropower plants in order to utilise as much resource from nature.

A hydropower plant consists of several components such as a valve, turbine, generator, etc. And one of such important components is the generator that converts mechanical energy to electrical energy. A generator needs an excitation system to provide field current to the field winding in order to induce the voltage in the generator terminal. An excitation system contains mainly an exciter that produces field current and an excitation control system that consists of an Automatic Voltage Regulator (AVR), controllers, and protective limiters to operate the generator and exciter within their capability in order to prevent destruction.

An AVR mainly controls field voltage, thereby the field current in order to obtain the desired output concerning the reference. Whereas, the controllers influence the AVR's reference to obtain the desired output, such as terminal voltage, power factor, or reactive power. The limiters influence the AVR to protect the generator by limiting the field and stator current to prevent the overheating of the field and stator winding, loss of synchronisms, and loss of excitation relays.

There are different type of conventional and specialised protective limiter has been used all over the world. This paper focuses on developing the conventional limiters to study their behaviour.

2 Theory

In order to understand the workings of the implemented limiters some basic theory knowledge is required. The following background information is mainly based on (Kundur, Balu, and Lauby 1994) and (IEEE 2016). A synchronous generator must be operated within its limits for active and reactive power output in order to not exceed the thermal capability of different components. The limiters ensure that exciters and synchronous generators are not exceeding their capability limits during normal and abnormal operating conditions. Therefore, the limiters comprise several types of control and protective functions. Most common limiters are determined using the generator capability curve (GCC) of a specific generator.

Figure 1 depicts the GCC of a synchronous generator, where curve A is a Field Current Overexcitation Limiter (FCOEL), also called Overexcitation Limiter (OEL), that limits the field current during the overexcited (exporting reactive power to the grid) operation. And curve B is a Stator Current Underexitation Limiter (SCUEL), also called Underexcitation Limiter (UEL), that prevents the excitation level from falling below the limit concerning active and reactive power or current during the underexcited (importing reactive power from the grid) operation. Curves C represents stator winding limits that are protected by the Stator Current Limiter (SCL). The Volts-per-hertz limiter is another limiter being used to protect equipment in the power plant.

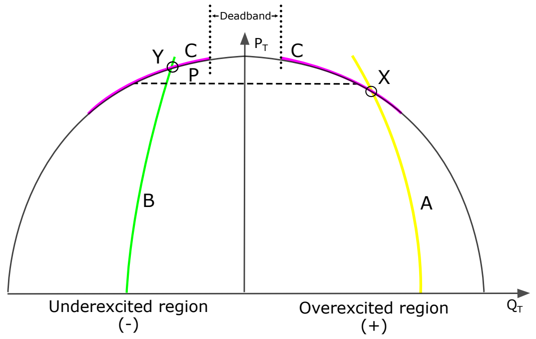

Figure 1. Synchronous generator capability curve with standard limits A: Field current limits, B: Stator end region limit and, C: Stator winding limit (between X and Y), and P: Turbine power (IEEE 2016)

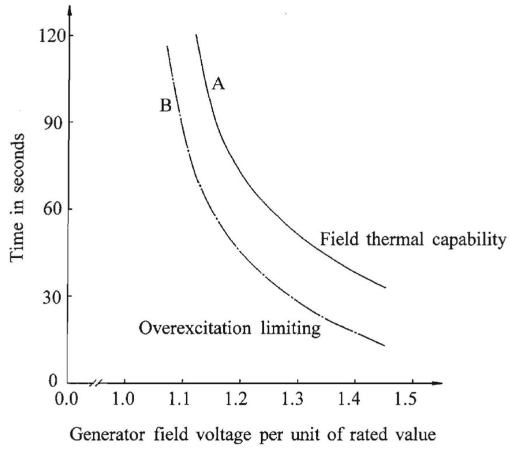

Figure 2. Coordination of overexcitation limiting with field thermal capability (Kundur, Balu, and Lauby 1994)

2.1 Field Current Overexcitation Limiter (FCOEL)

The field current overexcitation limiter protects the generator from overheating due to prolonged field overcurrent. Simultaneously, it allows the maximum field forcing for power system stability purposes. The generator field winding is designed to operate continuously at rated load conditions. But during voltage collapse or system islanding, the power system will be stressed and cause the generator to operate at high levels of excitation for a period. This limiter measures the field current, field voltage, or exciter field current or voltage to detects overexcitation. When the overexcitation is detected, it allows continuing the overexcitation for a certain period, defined as the time-overload period, and then reduce the excitation level to a safe level. If this function does not reduce the excitation to a safe value, the FCOEL limiter will trip the exciter field breaker.

The FCOELs have two types of time-overload periods that allow overexcitation, inverse time or fixed time. The inverse time limiters operate with the time delay matching the generator's field thermal capability, as shown in Figure 2. While the fixed time limiters operate when the field current exceeds the pickup value for a fixed set time, irrespective of the degree of overexcitation. Currently, a more common type of FCOEL is a combination of both instantaneous and inverse-time pickup characteristics.

2.2 Stator Current Underexcitation Limiter (SCUEL)

The Stator current underexcitation limiter prevents the reduction of the excitation level of the synchronous generator by increasing the excitation in the generator for one or more following purposes:

- To prevent operating beyond the small-signal (steady-state) stability limit of the synchronous generator, which could lead to loss of synchronism.
- To prevent loss-of-excitation relays from operating during underexcited operation.
- To prevent overheating in the stator end region of the synchronous generator, typically defined by GCC.

The SCUEL typically uses a combination of either voltage and current or active and reactive power of the synchronous generator to determine the control signal. Most importantly, the limiter should be coordinated with the required protection purposes as mentioned above in order to protect the generator properly. Figure 3 demonstrates a coordination of the calculated small-signal stability limit (I) and loss- of-excitation relay characteristic (II), where the intention was to protect against small-signal stability (I). If the UEL is supposed to protect against overheating in the stator end region, the coordination will be the same, but the small-signal stability limit is replaced by the overheating limit.

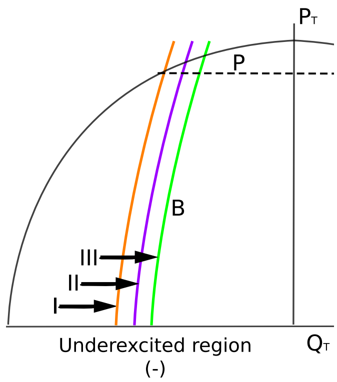

Figure 3. Coordination between UEL. I: Small-signal stability limit, II: Loss-of-excitation relay, III: Underexcitation limit set by the UEL, and P: Turbine power (IEEE 2016)

2.3 Stator Current Limiter (SCL)

A Stator current limiter is used to limit the high stator currents that cause overheating of the stator winding. High stator currents may occur due to significant changes in

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system voltage or increase in turbine power without considering the capability of generator stator windings. Here the SCL cannot directly limit the generator output current (stator current); it can only modify the field excitation during the operation with reactive stator current. As another option, tab change of the main transformer or reduction of turbine power can be considered to reduce the stator current.

Common SCLs mainly vary the excitation level to limit the stator current. The excitation level is varied based on whether the synchronous generator is operating inside the overexcited or underexcited region. When the generator is overexcited, the SCL should reduce the excitation in order to reduce the stator current, while when the generator is underexcited, the SCL should increase the excitation to reduce the stator current.

The SCL is responsible for limiting the stator current between points X and Y on the GCC, as shown in Figure 1, where the SCL's limit or set-point should be below the OEL's predefined limit and above the UEL's predefined limit. In addition, the SCL set-point is usually set above the stator current corresponding to generator-rated apparent power to ensure that the SCL does not reduce the excitation during the normal operation. Most commonly, the turbine capability limits the active power output of the generator in such a way, the reactive power output remains below the SCL characteristic. Thereby, the SCL would never become active under normal voltage conditions. But, if the turbine power increases, the generator stator windings should be upgraded. Otherwise the SCL might become active under normal operating conditions.

2.4 Volts-per-Hertz (V/Hz) Limiters

V/Hz limiters protect the generator's core and step-up transformers from significant overheating and damage due to excessive magnetic flux. The excessive magnetic flux typically results from low frequency and/or over-voltage. This limiter calculates the ratio of per unit voltage and per unit frequency and controls the field voltage to limit the generator voltage when the V/Hz value exceeds a preset value. The volts-per hertz limiters trip the generator by shutdown the field voltage when the V/Hz value exceeds the preset value for a certain period. V/Hz limiter usually has two grades of settings, where one with a higher V/Hz and shorter time settings, and another with a lower V/Hz and longer time settings. This is due to terminal limitations of the generators and step-up transformer.

3 Modelling of Limiters

This section gives an overview of the modelling of protective limiters based on (Kundur, Balu, and Lauby 1994) and (IEEE 2016). In addition, it provides information about implemented user interfaces in the models using Modelica. Indeed, most variables name and their descriptions in each model originate in the IEEE Std 421.5-2016 (IEEE 2016). However, some variables names and descriptions are modified for modelling purposes. Moreover, all the model's inputs are in the per-unit except the frequency which is Hz.

3.1 Field Current Overexcitation Limiter (FCOEL)

The FCOEL, modelled based on *OEL2C* in IEEE Std 421.5-2016 (IEEE 2016) shown in Figure 4, can interact with the Automatic Voltage Regulator (AVR) either as an addition to the summation point or at the takeover junction. If the FCOEL model is connected to the summation point, the maximum output limit should be set to zero, while the minimum output limit should be set to a negative value corresponding to the maximum reduction. Unlike when the FCOEL is connected to the takeover junction, the maximum output limit of the FCOEL should be set to larger values, whereas the minimum output limit should be set to a positive value that maintains the minimum excitation level. And the input to the limiter could be the generator field current I_{FD}, generator field voltage E_{FD}, or a signal proportional to exciter field current V_{FE}.

Besides, the FCOEL's output is limited by the PID controller's maximum and minimum limit if the lead-lag function is turned off; otherwise, the output is limited by $V_{\text{FCOELmax1}}$ and $V_{\text{FCOELmin1}}$ or $V_{\text{FCOELmax2}}$ and $V_{\text{FCOELmin2}}$.

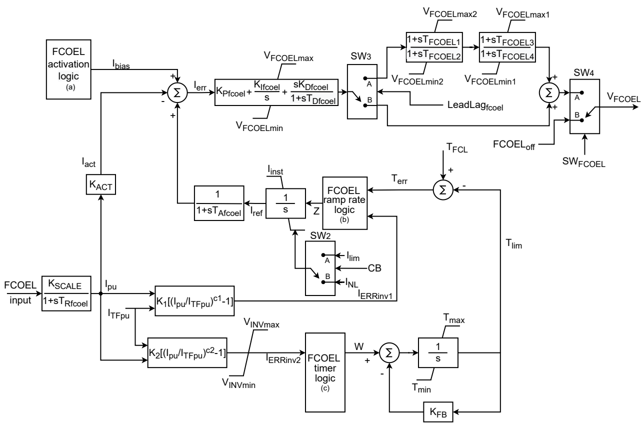

Figure 4. Block diagram of the field current overexcitation limiter (FCOEL)

The activation logic (a) in Figure 4 allows the user to specify an activation delay time T_{enFCOEL}, this time delay will disable the instantaneous FCOEL responses for a certain time to allow very high transient forcing capability. Also, it allows defining time delay to reset the limiter and reset threshold value.

When the timer error signal T_{err} = T_{FCL} - T_{lim} is less or equal than zero, or if the actual feedback field current I_{act} is greater equal than the reference I_{ref} for longer or equal than the activation delay time T_{enFCOEL}, or if the T_{enFCOEL} is equal to zero, then the output of the activation logic I_{bias} becomes zero.

Thus, the error I_{err}, the input to the PID controller is reduced, and consequently, the output of the FCOEL V_{FCOEL}

reduces towards the limiter minimum until the field current reaches the preset limit. The preset limit could be instantaneous field current limit I_{inst}, or thermal (long-term) value I_{lim} or no-load limit I_{NL} level. While, when the I_{ref} is less-equal than I_{inst} and the error $(I_{ref} - I_{act})$ is larger or equal than the reset-threshold value $I_{\mathrm{THoffFCOEL}}$ for longer or equal than the reset time delay T_{offFCOEL}, then the output I_{bias} becomes the reset reference value $I_{\mathrm{resetFCOEL}}$. As a consequence, the output V_{FCOEL} will reach back to maximum limits set by the PID controller or double lead-lag function.

This model comprises both instantaneous and timed responses, where the timed response could follow fixed ramp rates or inverse-time. The inverse-time characteristic of the FCOEL is calculated using the actual field current I_{pu} and parameters (K_2, c_2, and I_{TFpu}), and then the output signal I_{ERRinv2} is applied to the timer logic (c) in Figure 4. The inverse-time characteristic can be disabled by either set the parameter K_2 to zero or by setting the limits V_{INVmax} and V_{INVmin} to zero. The timer logic determines the input signal to the timer integrator by using defined fixed time ramp rates, $Fixed_{ru}$ and $Fixed_{rd}$ together with I_{ERRinv2}. Whereas the timer integrator output T_{lim} and fixed-parameter T_{FCL} determine the timed action of FCOEL.

The ramp rate logic (b) in Figure 4 uses the T_{err} signal to determine if the reference field current I_{ref} should be ramped up to the I_{inst} value or ramped down to the I_{lim} or I_{NL}. The ramp rate can be constant values as K_{ru} (ramp-up) and K_{rd} (ramp-down) or can be given by I_{ERRinv1}. Where the signal I_{ERRinv1} is calculated similarly to I_{ERRinv2} with parameters (K_1,c_1, and I_{TFpu}). Switching from instantaneous limit I_{inst} to timed limit $I_l im$ or I_{NL} is constituted by setting the SW_1 to false and K_{ru} and K_{rd} to large values. But, if it is a desire to have a ramp down at a rate calculated from overexcitation can be obtained by setting the SW_1 to "true" and select a proper parameter for K_1 and c_1. During the no-load condition (circuit breaker is in the open position), the switch SW_2 is changed to position "B", meaning the lower limit of the integral to the no-load limit I_{NL}. Otherwise, during the normal operating condition (circuit breaker is in the closed position), the lower limit is set to I_{lim}.

There are PID and double lead-lag at the output of the FCOEL, which determine the FCOEL's dynamic response. If PID control is desired, the lead-lag functions can be disabled by changing the position of the switch SW_3 to "B". Alternatively, if the double lead-lag compensation is desire, the gain K_{Ifcoel} and K_{Dfcoel} should be set to zero, simultaneously the position of the switch SW_3 should be set to "A".

Finally, the switch SW_4 at the output of the FCOEL is used to switch off the limiter's output by the user command. Then the output of the FCOEL will be the user-defined parameter $FCOEL_{off}$. Figure 5 shows modelled FCOEL in Modelica, where the radio buttons are implemented to switch the SW_1 to alternate from fixed time ramp

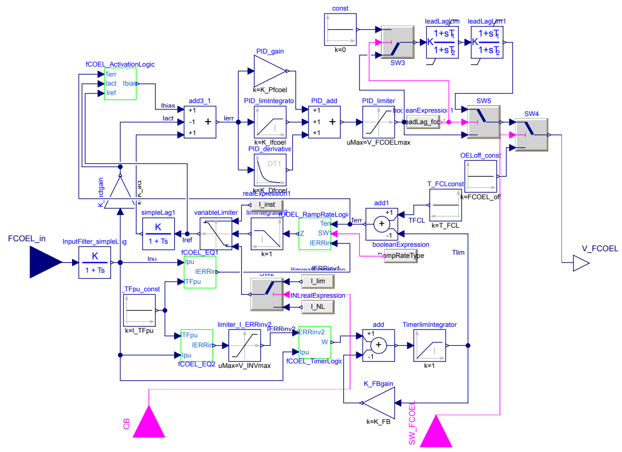

Figure 5. Implementation of Field current overexcitation limiter (FCOEL) in Modelica

rate to the calculated ramp rate from overexcitation. There is a checkbox named `LeadLag_fcoel` shall be checked to change the position in SW_3 to "A" in order to activate the lead-lag function. Moreover, the lead-lag should be enabled in order to parameterise the lead-lag function else the parameters boxes are locked.

3.2 Stator Current Underexcitation Limiter (SCUEL)

The block diagram of the SCUEL shown in Figure 6 is based on the type *UEL2C* in IEEE Std 421.5-2016 (IEEE 2016). The limiter senses the active power P_T and reactive current I_Q and increases the excitation when the generator runs at underexcitation below the defined characteristic value. Since the limiter is a separate circuit, the output signals of this limiter can interact either with the summing point or the High-value (HV) gate input of the excitation system. The interaction with the summing point leads to normal voltage control, whereas interaction with the HV gate (takeover junction) will overwrite the normal action of the AVR. Be aware that the inputs could also be the active current I_P instead of active power P_T, but it should be a positive value and also reactive power Q_T can be used instead of reactive current I_Q.

If the SCUEL interacts with the summation point, the minimum output limit should be set to zero, while the maximum output limit should be set to a large positive value. On the contrary, if the SCUEL is connected to the takeover junction, the maximum output limit of the SCUEL output should be set to 0, whereas the minimum output limit should be set to a significant negative value. Besides, the SCUEL's maximum and minimum limit is set by the PID controller's limit if the lead-lag function is turned off; otherwise, the output is limited by $V_{\mathrm{SCUELmax1}}$ and $V_{\mathrm{SCUELmin1}}$ or $V_{\mathrm{SCUELmax2}}$ and $V_{\mathrm{SCUELmin2}}$.

The voltage bias logic (a) in Figure 6 provides an adequate voltage ratio to be used in equation blocks F_1 and F_2. The logic can be bypassed by setting the parameter $V_{\mathrm{biasSCUEL}} = 1$. The equation blocks F_1 and F_2 in the

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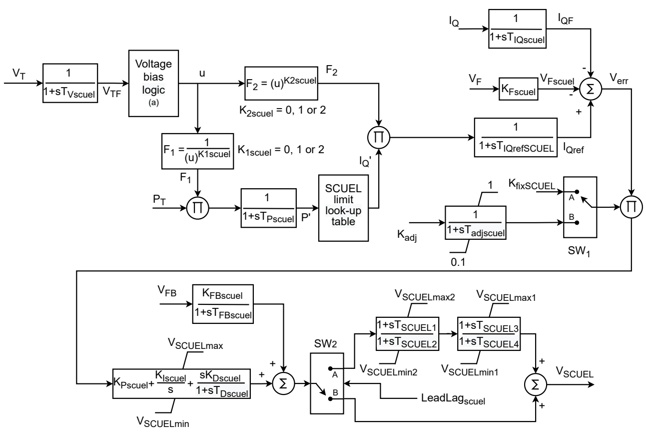

Figure 6. Block diagram of the Stator Current Underexcitation Limiter (SCUEL) (IEEE 2016)

SCUEL block diagram provide appropriate adjustments so that the effects of the terminal voltage V_T on the limiter are taken into account. The adjustments provided by the F_1 and F_2 are based on the limiting characteristics of the SCUEL and determined by the constants $K_{1\text{scuel}}$ and $K_{2\text{scuel}}$. If the SCUEL is configured to be influenced by the active and reactive currents, the limiter characteristic is set proportional to V_T by using the $K_{1\text{scuel}} = K_{2\text{scuel}} = 1$. While, if the limiter is influenced by the active and reactive components of the apparent impedance looking from the machine terminals, the characteristic can be set to proportional to the V_T^2 by using $K_{1\text{scuel}} = K_{2\text{scuel}} = 2$. However, the latter limiting characteristic requires proper coordination with generator protection functions such as loss-of-excitation relays. Also, this function can be disabled by using $K_{1\text{scuel}} = K_{2\text{scuel}} = 0$.

The SCUEL shown in Figure 6 takes the active power P_T and multiplies it by F_1, further filters it and the resulting normalised value P' is sent to the look-up table. The limiting characteristic defined in a lookup table determines the corresponding normalised reactive current value I_Q' related to P'. The reference I_{Qref} is determined by multiplying the I_Q' and F_2 and then compared with the filtered actual reactive current I_{QF}. If the error signal $V_{err} = I_{\text{Qref}} - I_{\text{QF}} - V_{\text{Fscuel}}$ becomes negative under the normal condition, the limiter's output will be the minimum PID or lead-lag limit, meaning no actions are taken. When the error signal becomes positive, the output of the SCUEL drives in the positive direction and boosts the excitation to move the operating point back towards the SCUEL limit.

The SCUEL reduction gain can be either automatically adjusted (depending on V_T, P_T and I_Q) or can have a fixed constant gain value. To be able to enable the automatically adjusted gain, the logic switch SW_1 should be selected to position "B", where the automatic adjustable gain reduction K_{adj} is calculated using Equation 1, while the fixed constant gain, given by the parameter K_{fixSCUEL} value, is enabled by switching the SW_1 to position "A". The gain reduction can be disabled by setting $K_{\text{fixSCUEL}} = 1$.

$$K_{adj} = \frac{\dfrac{V_T^2}{X_q} + I_Q}{\sqrt{(\dfrac{V_T^2}{X_q + I_Q})^2 + P_T^2}} \tag{1}$$

where

K_{adj}:	Automatic adjustment gain	[-]
V_T:	Generator terminal voltage	[pu]
P_T:	Active power	[pu]
I_Q:	Reactive current	[pu]
X_q:	q-axis synchronous reactance	[pu]

The excitation stabiliser signal from the AVR shall be provided to the input V_F, and it helps to damp the oscillations. The input V_{FB} can only be used in conjunction with the excitation system ST7C model. As mentioned earlier, the lead-lag blocks can be disabled by changing the position of the switch SW_2 to "B", and PID control by set gain K_{Iscuel} and K_{Dscuel} to 0. Besides, if the lead-lag function is desired, change the SW_2 to position "A", and the time constants should be appropriately adjusted to provide sufficient damping. The limiting characteristic of the SCUEL is depicted in Figure 7, where the limit is composed of four straight line segments. All five endpoints should be defined in terms of P_i and I_{Qi} values in order to determine the limiter characteristic. For any values of P', the corresponding value of I_Q' between the segment endpoints is determined using linear interpolation.

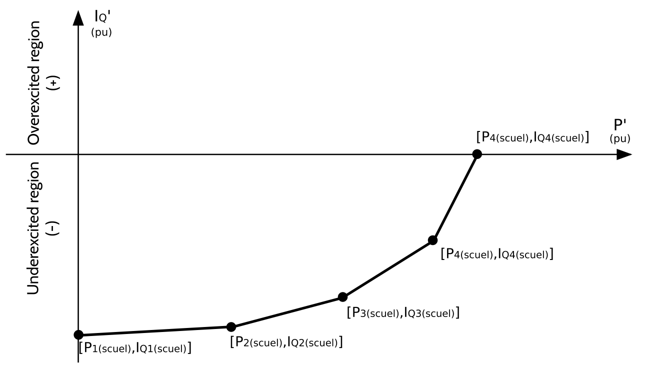

Figure 7. Normalised limiting characteristic for the SCUEL (IEEE 2016)

Figure 8 displays the modelled SCUEL in Modelica. There are two checkboxes implemented, one that changes the position of SW_2 from "B" to "A", while the other one alternates the switch from position "A" to "B" in order to enable the adjustable gain reduction, by checking it. Additionally, by enabling the lead-lag function and adjustable gain reduction, the parameter boxes will be enabled to allow the user to define corresponding parameters; otherwise, the parameter boxes are locked. Besides, when the automatically adjustable gain reduction is enabled, the parameter box for K_{fixSCUEL} will be locked. Alternatively, by unchecking the checkbox, the parameter box for the fixed

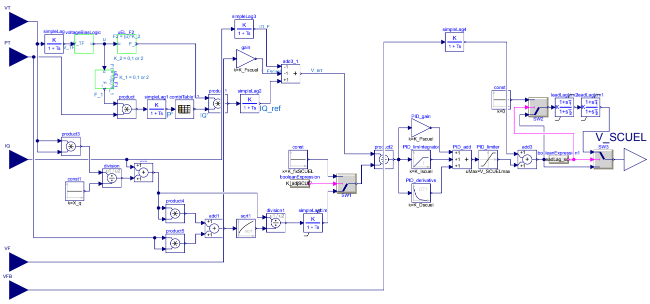

Figure 8. Implementation of Stator current underexcitation limiter (SCUEL) in Modelica

gain K_{fixSCUEL} will be opened, and the switch is back to the position "A".

3.3 Stator Current limiter (SCL)

A stator current limiter modifies the excitation level to reduce the reactive component of the stator current; as a consequence, the stator current will be limited. Figure 9 shows a block diagram of the SCL based on the type *SCL1C* in IEEE Std 421.5-2016 (IEEE 2016). This limiter uses the stator current I_T, reactive current I_Q, and reactive power Q_T at the generator terminal as inputs. Further, the output signal V_{SCL} from the SCL can only interact with the summing point of the excitation system.

When the magnitude of the I_T becomes greater than the adjustable pick-up value I_{SCLlim}, then the SCL starts to influence the excitation after the time delay. The time delay before limiting allows a short-term increase of stator current during a system disturbance or startup. There are three types of time delay functions implemented in this limiter. One of the time delay functions caused by the transducer delay in the measurement of the stator current is represented by the time constant T_{IT}. The second and third type time delay functions are enabled if the switch SW_1 on position "B", and the time delays are determined by an inverse time characteristic T_{INV} or a fixed-time T_{DSCL}. The switch SW_2 in the delayed reactive power logic (c) in Figure 9 should be set to "true" to enable the inverse time delay; else, the fixed-time delay will be applied.

A deadband is implemented at unity PF because the SCL does not affect the active power, so modifying the excitation level does not give any benefits at unity PF. There are two options to provide the deadband to the limiter; if the reactive current is used to modify the excitation, the deadband zone can be defined by the parameter I_{Qmin}. Whereas if the reactive power is used, then the deadband can be defined by the parameter V_{SCLdb}.

When the SW_1 is in position "A", the reactive current is used to determine if the generator is operating in an overexcited or underexcited condition. When the SW_1 is in position "B", the reactive power is used to determine the generator's operating condition. During the underexcited condition, the excitation current is increased, unlike during the overexcited condition, the excitation current is decreased.

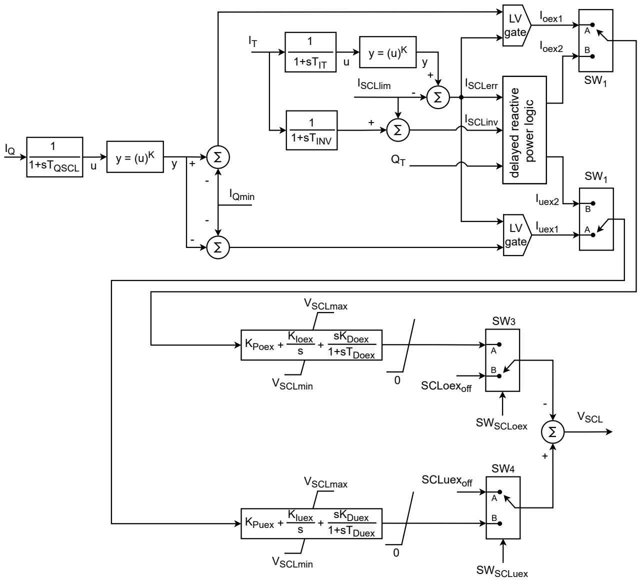

Figure 9. Block diagram of the stator current limiter (SCL) (IEEE 2016)

There are two individual PID controllers for overexcited and underexcited control loops, which can be individually adjusted for proper tuning of the PID controllers. If I_Q or Q_T within the deadband, the input to the PID controller becomes zero, and the PID controller's output will be held constant. Also, during the normal operation condition (when the I_T is lower than the I_{SCLlim}), the outputs of the overexcited and underexcited range will be zero; consequently, the output of the output V_{SCL} will be zero. When the I_T is higher than the I_{SCLlim}, the output V_{SCL} reduces during the overexcited range, while V_{SCL} increases during the underexcited range. However, under both ranges, the output decreases or increases until the reactive current or power reaches the deadband zone or until the I_T or Q_T becomes equal to the I_{SCLlim}. And there are two switches SW_3 and SW_4 at the output of the overexcited and underexcited range used to switch off each range's output, respectively, where the user shall give the command. When the outputs of the overexcited and underexcited range are switched off, the user-defined parameters `SCLoex_off` and `SCLuex_off` will be the output of each region, respectively.

The modelled stator current limiter in Modelica is displayed in Figure 10, where the switches at the output SW_3 and SW_4 should have a Boolean signal to enable the limiter's output.

Furthermore, there are implemented radio buttons for the switches, SW_1 and SW_2. If the radio button called "Reactive current controller" is selected, then the SW_1 is changed to position "A". Whereas, if the "Reactive power controller" radio button is selected, then the SW_1 is shifted to position "B", and the SCL uses the reactive power to determine the operating condition of the generator. As well, the switch SW_2 can be set to "true" by selecting the radio

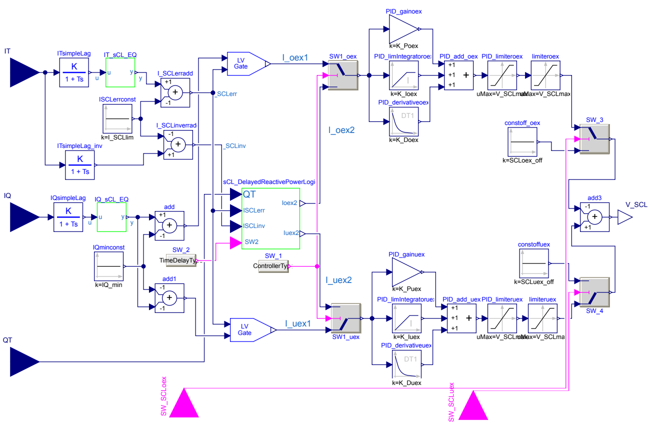

Figure 10. Implementation of stator current limiter (SCL) in Modelica

button “Enable inverse time delay”, while it can be set to “false” by selecting the “Enable fixed-time delay”.

3.4 Volts-per-Hertz (V/Hz) Limiter

V/Hz limiter is a voltage limiter that limits the voltage function of frequency. This model is build based on (Kundur, Balu, and Lauby 1994) and interacts with the AVR at the summing point, and reduces the reference so that the terminal voltage reduces with respect to the frequency reduction. A block diagram of the V/Hz limiter is shown in Figure 11, where the limiter takes inputs as terminal voltage V_T and frequency f. The limiter calculates the ratio between the terminal voltage and the frequency in per unit, which then is compared with the limiting value V_{ZLM} to determine the error E_{rr}.

If the E_{rr} is greater than zero, a timer will start to count, and when the time is greater than T_d, the E_{rr} signal will be sent further to the PID controller. During the normal operation (when the limiter us inactive), the E_{rr} is negative and thus, the output is zero; while when limiter is active and the E_{rr} becomes greater than the zero, the output starts to increase until the voltage reduces and the E_{rr} becomes less-equal than the zero. Additionally, this limiter can be activated and deactivated by the Boolean signal, and when the limiter is deactivated, the output will be zero.

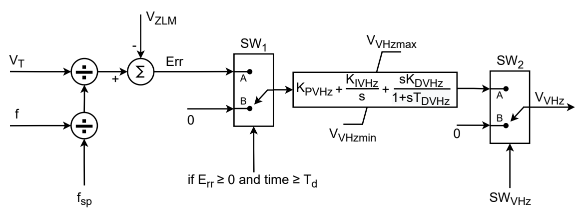

Figure 11. Block diagram of the volts-per-hertz (V/Hz) limiter (Kundur, Balu, and Lauby 1994)

A V/Hz limiter modelled in Modelica is shown in Figure 12, where the dashed lines illustrate the conditional connections that the user can activate either the constant frequency set-point f_{sp} or variable frequency set-point f_{vsp}.

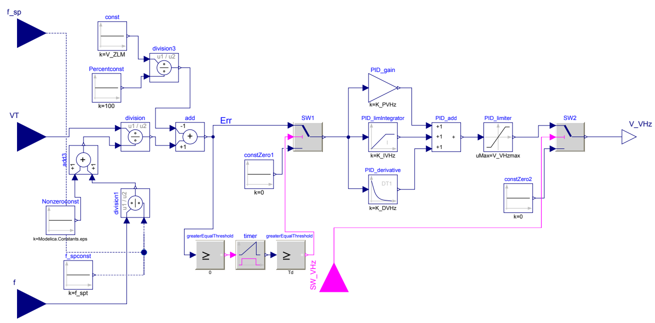

Figure 12. Implementation of V/Hz limiter in Modelica

There is a checkbox called `Enable_fvsp` implemented. By checking the checkbox the real input f_{vsp} is enabled so the variable frequency input can be connected to the limiter, and simultaneously the f_{sp} will be disabled. When the checkbox is unchecked, the f_{vsp} real input dissipates, and the f_{sp} is enabled. Additionally, the switch SW_2 at the output allows the user to activate and deactivate the limiter by a Boolean signal. Besides, a constant epsilon is added with the frequency to protect against division by zero problems.

4 Simulations Results

This section presents simulation results of Field Current Overexcitation Limiter (FCOEL), Stator Current Underexcitation Limiter (SCUEL), Stator Current Limiter (SCL), and the Volts-per-Hertz limiter (V/Hz).

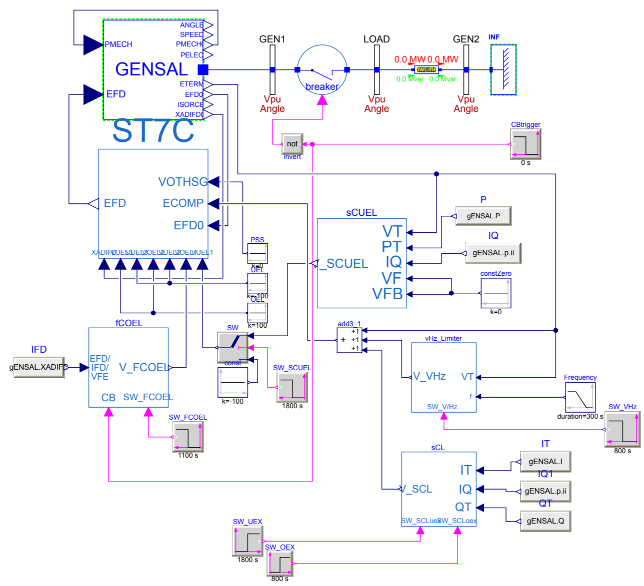

Figure 13. Test setup

The test setup is created using a GENSAL generator, transmission line, infinite grid, and excitation system type *ST7C* from the OpenIPSL version 2.0.0 (ALSETLab et al. 2018), as shown in Figure 13. The system power base and frequency for all the components are set to $10\,MVA$ and $50\,Hz$, accordingly. The generator is initialised, as presented in Table 1, during the various simu-

Table 1. Initialisation of GENSAL generator for simulation

Parameters	*Description*	*Values*	*Units*
P_0	Initial active power	-	MW
Q_0	Initial reactive power	-	Mvar
v_0	Initial voltage magnitude	1	pu
$angle_0$	Initial active power	0	◦
ω	Initial active power	0	pu

lations. Since the initial active power P_0 and the reactive power Q_0 will be varied for different simulation tests, the values are not presented in the table.

4.1 Field Current Overexcitation Limiter (FCOEL)

The test is performed by enabling the limiter output at 1100 s and open the circuit breaker at 2500 s.The initial active power P_0 and reactive power Q_0 of the generator are set to $8\,MW$ and $6\,Mvar$, accordingly.

The test results of the field current overexcitation limiter are presented in Figure 14. After the startup, the generator field current I_{FD} is stabilised to $2.15\,pu$, but the output of the FCOEL V_{FCOEL} is continuously at 100. When the limiter output is activated, the field current is limited to $I_{lim} = 1.95\,pu$, and consequently, the V_{FCOEL} reduces. Further, when the circuit breaker opens, the field current is limited to $I_{NL} = 1.07\,pu$, as desired.

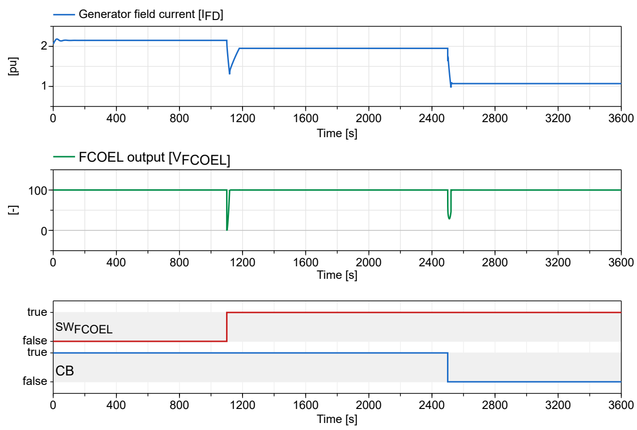

Figure 14. Field current overexcitation limiter (FCOEL) performance

4.2 Stator Current Underexcitation Limiter (SCUEL)

There is a switch manually added to the output of the SCUEL to control the output of the limiter (see Figure 8). The switch's position is set to change at $1800\,s$ to enable the output of the SCUEL. The initial active power P_0 and reactive power Q_0 of the generator are set to $7.5\,MW$ and $-4\,Mvar$, respectively, during the SCUEL simulation test. Besides, the inputs V_F and V_{FB}, are set to zero due to a lack of outputs from the *ST7C* model.

Initially, the limiter output is not connected to the AVR and the reactive current I_Q in a steady-state around $-0.36\,pu$, while the underexcitation I_Q limit is set to $-0.25\,pu$ at $0.75\,pu$ active power P_T. As a result, the limiter tries to increase the field current by increasing the output of the limiter towards the maximum limit (see Figure 15). When the limiter output is connected to the AVR at $1800\,s$, the limiter gradually decreases the output; hence the reactive current increases, and it ends up at $-0.25\,pu$, as expected. The output of the limiter is decreased and stabilised to a signal value of -99.98.

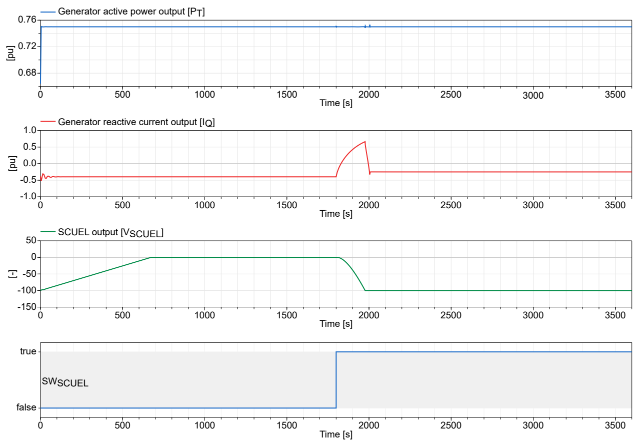

Figure 15. Performance of stator current underexcitation limiter (SCUEL)

4.3 Stator Current limiter (SCL)

The simulation test for the SCL is performed in two operational regions, inside the overexcited and the underexcited region. Both regions have separate PID controllers to operate under each region. As mentioned in subsection 2.3, SCL also consists of two types of controllers, reactive current and reactive power controllers. And each controller is also examined under each operational region. The output of the overexcited and underexcited regions is controlled by the Boolean input signals SW_{OEX} and SW_{UEX}, respectively, and these are set to "true" at 800 and $1800\,s$. In order to obtain generator terminal current IT above the pickup level I_{SCLlim} during the overexcited region, the initial active power P_0 and reactive power Q_0 of the generator are set to $8\,MW$ and $8\,Mvar$, accordingly. Whereas during the underexcited region test, only the initial reactive power Q_0 of the generator is changed to $-8\,Mvar$. In addition, the reactance of the transmission line X is set to zero during the simulations.

Figure 16 shows the performance of SCL during the overexcited region, where the solid lines illustrate reactive power controller performance while the dashed lines illustrate reactive current controller performance. Both controllers are simulated with similar parameters, except that each controller's proportional and integral gain are

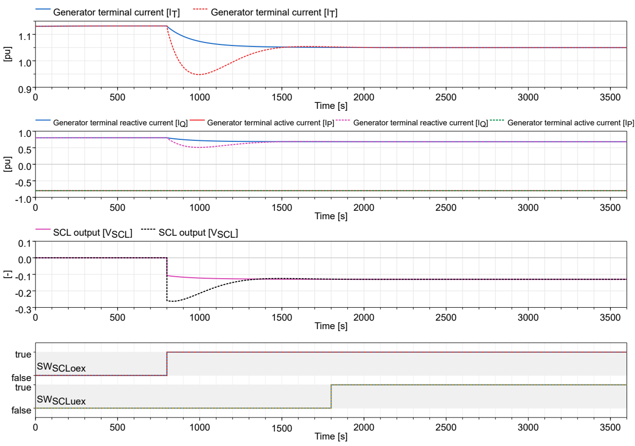

Figure 16. Test setup for stator current limiter (SCL) model

tuned separately to secure proper limitations. Note that the PID controller should be tuned separately for the reactive power and current controller. The overexcited region's output is enabled at 800 s, whereas the underexcitation region's output is enabled at $1800\,s$. The stator current limiter output V_{SCL} is reduced immediately after the overexcitation output is enabled and causes the field current to be reduced. As a consequence, the reactive power or current output of the generator reduces, thereby the generator terminal current I_T to reduced from $1.11\,pu$ towards the threshold value of $1.05\,pu$, as anticipated. However, enabling the output of the underexcitation region does not cause any reasonable changes. Furthermore, there is a notable difference between the performance of the reactive power and the current controller. As the results show that the reactive power controller reduces the terminal current smoothly; thereby, the overshoot that occurs during the reactive current control is eliminated.

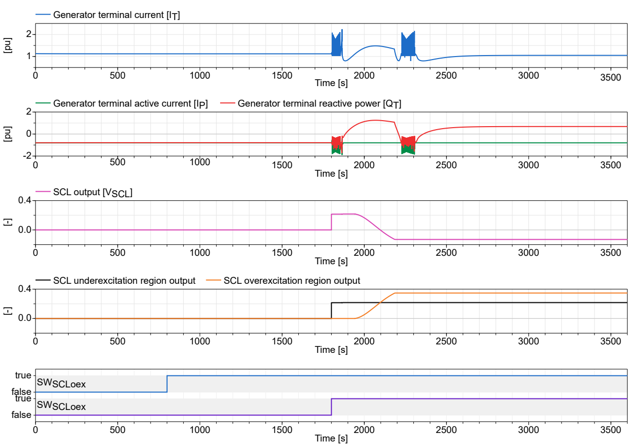

Figure 17. Test setup for stator current limiter (SCL) model

The simulation results of the reactive power controller in SCL during the underexcited condition are illustrated in Figure 17. The test is performed similarly to the overexcitation simulations when the Boolean signal SW_{UEX} turns "true" at $1800\,s$, the output V_{SCL} is increased, and causes the reactive power to increase into the overexcitation region. Hence, the SCL overexcitation part takes control of the reactive power and reduces until the terminal current reaches within I_{SCLlim}, as desire. There are some oscillations when the reactive power starts to increase into the overexcitation region as well as when the reactive power is reduced into the underexcitation region. The simulation results of the reactive current controller of SCL during the underexcited condition are not presented due to the random oscillations.

4.4 Volts-per-Hertz (V/Hz) Limiter

There is a ramp logic that is connected to the V/Hz model that represents actual frequency and a Boolean signal input that controls the output of the limiter (see Figure 13). At $800\,s$, the Boolean signal turns "true", so the output of the V/Hz limiter gets enabled, and then at 1800 s, the ramp logic reduces the frequency from nominal frequency $50\,Hz$ to $45\,Hz$. The generator is initialised with parameters $P_0 = 8\ MW$ and $Q_0 = 5\,Mvar$.

Figure 18 illustrates the performance of the V/Hz limiter, where the terminal voltage in the steady-state at $1.086\,pu$ before the set-point changes. When the frequency reduces, the deviation between voltage and frequency will increase above the defined limit; thus, the limiter's output signal starts to increase. As a consequence, the voltage starts to decrease nicely and stabilised at $0.99\,pu$ as expected.

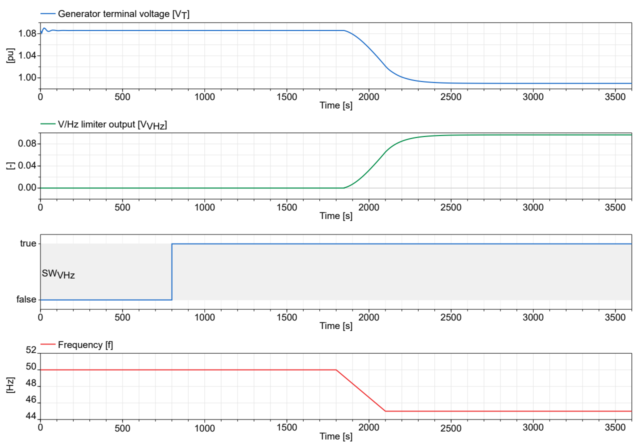

Figure 18. Performance of volts-per-hertz limiter

5 Discussion

This paper aims to model protective limiters Field current Overexcitation limiter (FCOEL), Stator current underexcitation limiter (SCUEL), Stator current limiter (SCL), and Volts-per-hertz (V/Hz) limiter in the Modelica modelling language. Fundamentally, the limiters are modelled based on IEEE Std 421.5-2016 (IEEE 2016); however, the models have been modified a bit due to modelling purposes and complexities. While the excitation system, type ST7C, is obtained from the OpenIPSL library, and the V/hz limiter is modelled based on Kundur (Kundur, Balu, and Lauby 1994).

Since the primary focus of this paper is to model the protective limiters, the test setup modelling is kept simple as possible to analyse the modelled excitation control system's performance. However, it should be properly modelled in the future for better examination of the model's performance.

According to IEEE Std 421.5-2016 (IEEE 2016), the lead-lag function in FCOEL and SCUEL could be disabled by setting their time constants to zero; however, it causes errors during the simulations; thus, those time constants are set to constant epsilon to be able to simulate. Despite this, the simulations failed randomly; this problem is solved by adding the switches to bypass the control signal from the PID controller to the output.

A PID controller is implemented in SCUEL and SCL, even if it is not stated in IEEE Std 421.5-2016 (IEEE 2016), in order to provide the user access to tune the controller's output properly.

According to IEEE Std 421.5-2016 (IEEE 2016), one of the FCOEL inputs could be generator field voltage E_{FD} as described in subsection 2.1, but during the simulations, using the E_{FD} as an input cause simulation error. The reason could be that in the FCOEL model, the signal I_{act} obtained from the input and connected to the output, causing algebraic loop. But the simulation error may be eliminated by adding a delay in the signal I_{act} or at the input.

The V/Hz limiter model is fundamentally modelled based on Kundur (Kundur, Balu, and Lauby 1994) as described in Section 2.4; however, simulation results showed that the model's behaviour was not desirable. Hence, the lead-lag function of the limiter was replaced by the PID controller, and the gains were removed to get a reasonable behaviour.

The overall behaviour of all the models was reasonable; be aware that the proportional and the integral gain of the FCOEL is relatively high, and the reason is not apparent yet; however, the model works as desire.

There are some oscillations when the reactive power starts to increase into the overexcitation region as well as when the reactive power is reduced into the underexcitation region (see Figure 17); the reason could be that the test grid is not adequately modelled in order to tackle the high current underexcitation operation. The simulation results of the reactive current controller of SCL during the underexcited condition are not presented in subsection 2.3 due to the random oscillations for the same reason as mentioned before. The SCL model should be further analysed in the future with a proper grid model to avoid unwanted oscillations. Further, by reflecting on the SCL's simulation results, the power controller may be the desired controller since it has the advantage of time delay and deadband, also work smoothly. However, better and smooth control of the reactive current controller could be achieved by better tuning of the PID controller.

The FCOEL, SCL, V/Hz limiters models have a switch at the output to disable the control function. These switches are used to enable the output during the simulation, which results in a sudden change in the control signal. This sudden increase in the control signal also impacted for example, field current, active power, or reactive power output. The main reason might be explained that the PID controller pushed the maximum control signal to the output, and the output signal does not make any changes in the system; therefore, when the switches enable the outputs, the maximum control signal is applied instantaneously. One possible way to fix this problem is by adding a self-reset function for the PID controller to reset when the output disables.

6 Conclusions

In this paper, the excitation control system's limiters are mainly object-oriented modelled in Modelica modelling language using Dymola software. The models are fundamentally modelled with reference to IEEE Std 421.5-2016 (IEEE 2016) and Kundur (Kundur, Balu, and Lauby 1994).

The limiters Field current overexcitation limiter (FCOEL), Stator current underexcitation limiter (SCUEL), Stator current limiter (SCL), and Volts-per-hertz (V/Hz) limiter were modelled separately from scratch, except the AVR, obtained from the external library OpenIPSL. Later, the models mentioned above were simulated separately and then compared to these controller's and limiter's theoretical behaviour.

In conclusion, all the models performed as desired but still need proper tuning and further development to enhance the performance. For the future it is planned to run further tests with real power plant data in order to improve and verify the behaviour of the limiter models.

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